## AMENDMENTS

### In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (previously presented) A protection circuit for protecting integrated semiconductor active devices from damage due to ESD voltages appearing on the circuit power bus lines said circuit comprising:

at least one switching circuit string composed of a first and second NMOS device and a PMOS device , wherein the gate of said first NMOS device is connected to a first voltage source and the drain element of said first NMOS device is connected to said active devices input/output signal pad and to the drain element of said PMOS device, and the source of said first NMOS device is connected to the drain element of said second NMOS device and the gates of said second NMOS and said PMOS are connected to an internal circuit and the source of said second NMOS is connected to a second voltage source, and the source of said PMOS is connected to a first voltage source; and

a protection discharging means for discharging ESD energy appearing between said first and said second voltage source, wherein said protection discharging means comprising a discharging NMOS device with a first and a second drain diffusion which extends under and around said first drain diffusion, the drain of said discharging NMOS device is directly connected to said first voltage source, and the source of said discharging NMOS device is directly connected to said second voltage source.

2. (original) The circuit according to claim 1 wherein said protection discharging means further comprises a resistor.

3. (cancelled)

4. (original) The circuit according to claim 2 wherein the gate of said discharging NMOS device is connected to the first end of said resistor and the second end of said resistor is connected to said second voltage source.

5. (original) The circuit according to claim 1 wherein said first drain diffusion is a N+ donor diffusion to form a normal NMOS drain region.

6. (previously presented) The circuit according to claim 1 wherein said special second drain diffusion is of opposite dopent than said first drain diffusion.

7. (original) The circuit according to claim 2 wherein said resistor has a value between 1 and 100 K ohms.

8. (original) The circuit according to claim 1 wherein said switching circuit string provides a driving current to said output pad.

9. (original) The circuit according to claim 1 wherein a value of said driving current is determined by the total number of said switching strings and whereby each said string can supply a current between 2 and 48 ma.

10. (original) The circuit according to claim 1 wherein said first voltage source is between 2.5 and 5 volts.

11. (original) The circuit according to claim 1 wherein said second voltage source is ground.

12. (currently amended) An effective Vcc to Vss power ESD protection device with reduced junction breakdown voltage connected between Vcc and Vss power bus lines comprising:

a substrate having a first dopent type;

isolation regions within said substrate for isolation of said ESD protection device;

a FET gate with abutting spacers for said ESD protection device;

multiple regions of a second dopent type of opposite dopent to said substrate for said ESD protection device between said gate and said isolation regions;

multiple regions of a third dopent type of opposite dopent to said substrate for said ESD protection device between said gate and said isolation regions;

a special fourth dopent region of similar dopent to said substrate under and around ~~beneath~~ one said second and third dopent region;

a protective insulation layer over said ESD protection device; and

first, second and third electrical conductor elements.

13. (original) The ESD protection device of claim 12 wherein said substrate is of P dopent with a concentration between 1E14 and 1E15 a/cm$^3$.

14. (original) The ESD protection device of claim 12 wherein said isolation regions are thermally grown to a thickness of between 4000 and 10,000 Å.

15. (original) The ESD protection device of claim 12 wherein said FET gate consists of gate oxide insulator between 70 and 350 Å in thickness and a polysilicon conduction element between 1500 and 4500 Å in thickness.

16. (original) The ESD protection device of claim 12 wherein said FET gate abutting spacers are of silicon oxide or silicon nitride.

17. (original) The ESD protection device of claim 12 wherein said multiple regions of second dopent type are N doped to a dopent concentration of between 1E16 and 1E18 a/cm$^3$.

18. (original) The ESD protection device of claim 12 wherein said multiple regions of a third dopent type are of N dopent with a dopent concentration of between 1E19 and 1E21 a/cm$^3$ and form the source and drain regions of a NMOS FET.

19. (original) The ESD protection device of claim 12 wherein said special fourth dopent region is doped with a P dopent with a dopent concentration of between 1E16 and 1E19 a/$cm^3$ and is located below and partially surrounding said NFET drain region.

20. (original) The ESD protection device of claim 12 wherein said drain electrical conductor element is connected to a first voltage source Vcc, and said source electrical conductor element is connected to a second voltage source, Vss or ground. resistor.

21. (original) The ESD protection device of claim 12 wherein said gate electrical conductor element is connected to the first end of a diffused resistor with a value between 1000 and 100000 ohms.

22. (original) The ESD protection device of claim 12 wherein the second end of said resistor is connected to said second voltage source Vss, or ground.

23. (previously presented) A method of forming a protection circuit for protecting integrated semiconductor active devices from damage due to ESD voltages appearing on the circuit power bus lines said method comprising:

connecting source region of a used PMOS device and the source and gate of an unused PMOS device to a first voltage source;

connecting the drains of said used and unused PMOS devices to said active devices input/output pad;

connecting the drain of said used PMOS device to a drain of a first used NMOS device, and the drain of said unused PMOS device to a drain of a first unused NMOS device;

connecting the gate of said used PMOS device and the gate of a second used NMOS device to separate logic signal lines;

connecting the gates of said first used and said first unused NMOS devices to said first voltage source;

connecting the source of said first used NMOS device to the drain of said second used NMOS device and connecting the source of said first unused NMOS device to the drain of a second unused NMOS device;

connecting the source of said second used NMOS and the source and gate of said second unused NMOS device to a second voltage source; and

connecting said ESD protection discharging means for discharging ESD energy appearing between and further directly connected to said first and second voltage source, wherein said ESD protection discharging means comprises a discharging NMOS device with a special diffusion region under and around said device normal drain region.

24. (canceled)

25. (original) The method according to claim 24 wherein said ESD protection discharging means is connected to the circuits to be protected by connecting said drain of said discharging NMOS device to said first voltage source and connecting the source of said discharging NMOS to said second voltage source.

26. (original) The method according to claim 24 wherein said ESD protection discharging means is connected to the circuits to be protected by connecting the gate of said discharging NMOS device to the first end of said resistor and connecting the second end of said resistor to said second voltage source.

27. (original) The method according to claim 24 wherein said special diffusion region under and around said discharging NMOS device normal drain region is created by an ion implant of boron with a dosage between 1E13 and 1E14 a/cm$^2$ and an energy of between 10 and 80 KeV, to produce a resultant dopent concentration of between 1E 16 and 1E19 a/cm$^3$.

28. (original) The method according to claim 23 whereby said first voltage source is generated to a positive level above ground designated Vcc with a value between 2.5 and 5 volts.

29. (original) The method according to claim 23 whereby said second voltage source designated Vss is connected to a voltage level below Vcc, typically ground.

30. (original) The method according to claim 23 whereby said separate logic signal lines are connected to internal logic devices.